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task distributing <near> MIPs values <near> DS   Search

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An 800-MOPS, 110-mW, 1.5-V, parallel **DSP** for mobile multimediaprocessing- seu.edu.cn [PDF]
H Igura, Y Naito, K Kazama, I Kuroda, M Motomura, ... - IEEE Journal of Solid-State Circuits, 1998 - ieeexplore.ieee.org
... targeted performance at reduced supply voltage—namely, 200 **MIPS** (800 MOPS ... (b)
Distribution of memory ... presented a parallel **DSP** that employs a **task**-level, coarse ...
Cited by 21 - Related articles - Web Search - BL Direct - All 5 versions

[PDF] ›Programmable **DSP** platform for digital still cameras
K Illgner, HG Gruber, P Gelabert, J Liang, Y Yoo, ... - IEEE INTERNATIONAL CONFERENCE ON ACOUSTICS SPEECH AND SIGNAL ..., 1999 - focus. ti.com
... The intensity **distribution** reflected from the scene is ... at low power consumption
(0.45mA/**MIPS**) [11 ... **Task** Cycles/Pixel Preprocessing (Black Clamping, Gain, White ...
Cited by 14 - Related articles - View as HTML - Web Search - BL Direct - All 4 versions

[PDF] ›A Scalable Real-time Signal Processor for Objectoriented Data Flow Applications
D Scherrer, H Eberle - Proceedings of the International Conference on Parallel and ..., 1998 - citeseerx.ist.psu.edu
... Figure 3: Example of an efficient **task distribution**. ... DRAM Peak performance:
400/530/(800) **MIPS** Switch bandwidth ... method calls do not have return **values** or output ...
Cited by 4 - Related articles - View as HTML - Web Search - All 6 versions

Technical challenges in the globalization of software radio
L Mitola III - IEEE Communications Magazine, 1999 - ieeexplore.ieee.org
... **DISTRIBUTION** Clock generation and **distribution** consumes a ... tationally intensive
software-radio **tasks** by exploiting ... programmability of such a **near**-term approach ...
Cited by 92 - Related articles - Web Search - BL Direct - All 2 versions

Method and apparatus to perform **task** scheduling
SH Lam - US Patent App. 10/669,309, 2003 - Google Patents
... f a processor based on the processor **task values** select 1 f ... may operate at a processing
speed of 100 **MIPS**. ... **task** scheduler 302 may per- form **task** scheduling for ...
Web Search - All 2 versions

Detector **array** control and triggering

S Aiello, A Anzalone, M Bartolucci, G Cardella, S ... - IEEE Transactions on Nuclear Science, 1998 - ieeexplore.ieee.org

... detector **arrays**, as in our case, **tasks** must be ... TMS320C30 **DSP** [II] (33.3 MFLOPS and
16.7 **MIPS**) ... is a function with a frequency **distribution** curve characterized ...

Cited by 10 - Related articles - Web Search - BL Direct - All 4 versions

Multiprocessor digital signal processing on Earth orbitingscatterometers

A Bachmann, D Clark, J Lux, R Sterne - Aerospace Conference, 2001, IEEE Proceedings., 2001 - ieeexplore.ieee.org

... scatterometer launched last year measures world wide **near** surface ocean wind ... for
a large number node system where **task** and resource **distribution** can become ...

Cited by 2 - Related articles - Web Search - All 2 versions

An application-tailored dynamically reconfigurable hardwarearchitecture for digital baseband ...

J Becker, T Pionteck, M Glesner - Integrated Circuits and Systems Design, 2000. Proceedings. ..., 2000 - ieeexplore.ieee.org

... of 384 kbps will require more than 6000 **MIPS**. ... These **tasks** can then be implemented
using already existing ... the next page the **distribution** of the different input ...

Cited by 14 - Related articles - Web Search - All 5 versions

Flexcc2: An optimizing retargetable c compiler for **dsp** processors

V Bertin, JM Daveau, P Guillaume, T Lepley, D ... - Lecture notes in computer science, 2002 - Springer

... Second, the irregularity of execution **distribution** in **DSP** algorithms ... a set of lowering
engines for this **task**. ... or source code modi- fications) is 18.6 **MIPS**. ...

Cited by 8 - Related articles - Web Search - BL Direct - All 4 versions

REAL-TIME IMPLEMENTATION OF G. 723.1 SPEECH CODER USING TMS320VC5402 **DSP** CHIP

M MOOSAVINEZHAD - Iranian Journal of Information Science & Technology, 2004 - srist.com

... The **task** is further complicated by the fact that ... Lee, Park and Jang analyze the
distribution of computational ... the pulse would be located **near** the neighborhood ...

Related articles - Web Search

Key authors: L Mitola - D Brooks - P Pirsch - P Bose - S Schuster

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MIPs values update with modulo <near> DSP a   Search

"with" is a very common word and was not included in your search. [details]

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Cost-effective implementation of ITU-T G. 723.1 on a **DSP** chip
SM Lee, S Park, Y Jang - Consumer Electronics, 1997. ISCE'97., Proceedings of 1997 ..., 1997 - ieeexplore.ieee.org
... t have zero **value**, the gain **value** was set ... in the search loop, maximum 17300cycles (
0.6**MIPS**) were saved ... response calculation, and filter memory **update** as shown ...
Cited by 4 - Related articles - Web Search

Method and apparatus to perform task scheduling
SH Lam - US Patent App. 10/669,309, 2003 - Google Patents
... of 100 may operate at a processing speed of 100 **MIPS**. ... In one embodiment, the **update**
operations may be described ... A second resource cost **value** for a second task ...
Web Search - All 2 versions

The dod 4.8 kbps standard (proposed federal standard 1016)
JP Campbell Jr, TE Tremain, VC Welch - Advances in Speech Coding, 1991 - books.google.com
... Table 1. CELP Characteristics **Update** Linear Predictor Adaptive ... independent) closed
loop 60 dimensional **mod** MSPE VQ ... Our **MIPS values** shouldn't be confused with ...
Cited by 77 - Related articles - Web Search

Flexcc2: An optimizing retargetable c compiler for **dsp** processors
V Bertin, JM Daveau, P Guillaume, T Lepley, D ... - Lecture notes in computer science, 2002 - Springer
... and use post- incremented/decremented addressing mode to **update** the pointer ... scheduling
microengines 9 . For comparison, we obtain a **value** of 52,8 **MIPS** with a ...
Cited by 3 - Related articles - Web Search - BL Direct - All 4 versions

Byte and **modulo** addressable parallel memory architecture for video coding
JK Tanskanen, T Sihvo, J Niittylahti - IEEE Transactions on Circuits and Systems for Video ..., 2004 - ieeexplore.ieee.org
... AltiVec [6], and Silicon Graphics **MIPS** V ISA ... once in one operation, the absolute
update value must be ... to the circular buffer size (**modulo value**), the circular ...
Cited by 13 - Related articles - Web Search - BL Direct - All 3 versions

Systematic high-level address code transformations for piece-wiselinear indexing: illustration on a ...
C Ghez, M Miranda, A Vandecappelle, F Catthoor, D ... - 2000 IEEE Workshop on Signal Processing Systems, 2000. SIPS ..., 2000 - ieeexplore.ieee.org
... different loops consistent, we need to **update** each pointer ... since they only depend
on the **values** ci, di ... these small **arrays** introducing many **modulo** operations and ...
Cited by 26 - Related articles - Web Search - All 4 versions

PID control with 32-bit RISC microprocessors
R Leach, M Inc, TX Austin - Northcon 95. I EEE Technical Applications Conference and ..., 1995 - ieeexplore.ieee.org
... **values** are combined to produce total **MIPS** required for ... and reducing data dependencies
by preloading **values** used by ... separated and the load with **update** must be ...
Web Search

A digital signal processor with IEEE floating-point arithmetic
GRL Sohie, KL Kloker, M Inc, TX Austin - IEEE Micro, 1988 - ieeexplore.ieee.org
... on assembly-language benchmarks averages 13 **MIPS** and 18 ... During a DMA transfer, one
modulo- address arithmetic unit ... IEEE encodings for 32-bit SP **values** have 1 ...
Cited by 26 - Related articles - Web Search - All 3 versions

Digital control for embedded applications

R Leach, M Inc, TX Austin - Southcon/96. Conference Record, 1996 - ieeexplore.ieee.org

... **values** are combined to produce total **MIPS** required for **...** and reducing data dependencies by preloading **values** used by **...** separated and the load with **update** must be **...**

Related articles - Web Search - BL Direct - All 2 versions

Memory organization for improved data cache performance in embedded processors - umd.edu [PDF]

PR Panda, ND Dutt, A Nicolau - Proceedings of the 9th international symposium on System ..., 1996 - portal.acm.org

... s CW4001 [2], which is based on the **MIPS** family of **...** edges to nodes in cluster C just formed **Update** S(V **...** When we have equal T **values** for multiple nodes, we select **...**

Cited by 47 - Related articles - Web Search - All 13 versions

Key authors: **D Chin** - **B Mathew** - **J Peters** - **H Taylor** - **J Campbell**

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